Design Intern, Harlow

Renesas is one of the top global semiconductor companies in the world. We strive to develop a safer, healthier, greener, and smarter world, and our goal is to make every endpoint intelligent by offering product solutions in the automotive, industrial, infrastructure and IoT markets. Our robust product portfolio includes world leading MCUs, SoCs, analog and power products, plus Winning Combination solutions that curate these complementary products. We are a key supplier to the world's leading manufacturers of the electronics you rely on every day; you may not see our products, but they are all around you.

Renesas employs roughly 21,000 people in more than 30 countries worldwide. As a global team, our employees actively embody the Renesas Culture, our guiding principles based on five key elements: Transparent, Agile, Global, Innovative, and Entrepreneurial. Renesas believes in, and has a commitment to, diversity and inclusion, with initiatives and a leadership team dedicated to its resources and values. At Renesas, we want to build a sustainable future where technology helps make our lives easier. Join us and build your future by being part of what's next in electronics and the world.

The Design Engineering team in Harlow is focused on the design, development and integration of our industry leading analogue & power devices.

We are looking for candidates who have interests that could include analog or mixed signal design. We highly value communication skills and the motivation to work as part of a global team. Candidates will work under the guidance of a mentor to assist in developing high performance products. This placement will enable you to work within a dynamic mixed signal design engineering team and improve your skills further by participating in all aspects of the development of Integrated Power Regulators, including architectural analysis, modelling, simulation, physical design and parasitic extraction. You will also be involved in assisting the team with bench evaluation of prototypes, providing insight into the development of an integrated product, from specification to silicon realization.

This position is for candidates that are available for either summer or full academic year placements. The minimum period is 8 weeks.